FPGA based Design and Implementation of Cascaded FIR Filter for ECG Signal Processing

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Abstract: Clean ECG (Electrocardiogram) is very important to detect many diseases. ECG signal can be corrupted by various noises in real time situations. ECG is mainly corrupted by Baseline wander noise, Powerline Interference noise, and EMG noise. These types of noise are present at different frequency range of ECG signal. There are various filtering techniques available for removing these noises. This paper proposes FPGA based implementation of Kaiser Window based Cascaded FIR (Finite Impulse Response) filter in which FIR High Pass Filter, FIR Band Stop Filter and FIR Low Pass Filter are cascaded. Proposed implementation can remove Baseline wander noise, Powerline Interference noise, EMG (Electromyogram) noise in a single stage. The ECG database has been taken from Physio.net. The proposed FIR filter has been synthesized and implemented on Virtex5 FPGA using Xilinx ISE 14.5.

Keywords: FPGA, ECG, Baseline Wander Noise, Powerline Interference Noise, EMG Noise.

Introduction

ECG (Electrocardiogram) is the electrical activity of our heart. The signal has 'P' wave, the noise sensitive 'QRS' complex and 'T' wave [1] as shown in fig. 1. Each 'P', 'QRS', 'T' waves have its own significance to convey important information of heart [1]. With the help of electrodes which placed on a patient's body, ECG signal can be recorded. During each heartbeat, electrodes detect the tiny electrical changes of the body-skin that arise from heart muscle depolarizing [2]. The recorded ECG signal having several types of noise [2] such as Powerline interference (PLI), Baseline Wander, Electromyogram (EMG). It is very important to get a clean and clear ECG for diagnosis of many diseases [2]. To get a noise free ECG, different filtering techniques are available [2]. The ECG mainly corrupted by:

Baseline Wander Noise: It may be caused by improper electrode connections, respiration, and sweat [3]. The ECG signal viewed on a screen appears to "wander" rather than being straight.

Powerline Interference Noise: It may be caused by inappropriate grounding of the ECG equipment [4].

EMG (Electromyogram) Noise: It may be caused due to shrinkage of muscles other than the cardiac muscles [3].

The frequency range of ECG signal is 0.5 - 100 Hz. The Baseline Wander Noise nearly in between 0.1 to 0.5 Hz, Powerline Interference Noise occurs at 50/60 Hz, and High Frequency Noise i.e. EMG (Electromyogram) is nearly in between 100 to 500 Hz. There are different filtering methods for removing these types of noise of ECG. This paper focuses on FIR (Finite Impulse Response) filter. FIR filter is simple to implement which requires multipliers, adders, registers.

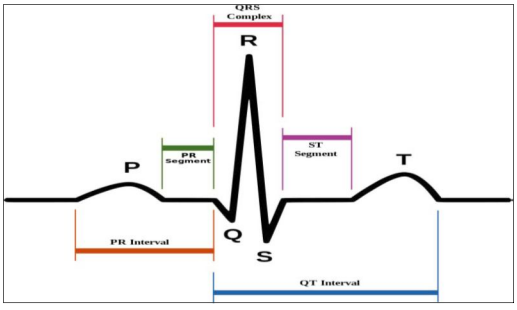

Figure1. A Typical ECG Signal [5]

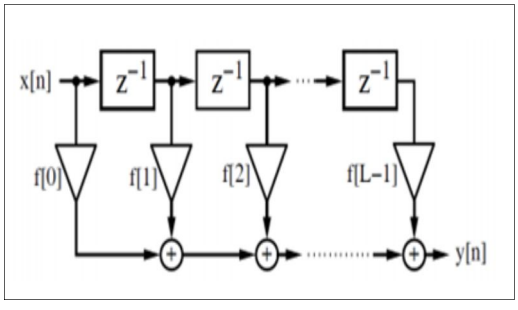

Figure2. Structure of FIR filter [6]

The general difference equation is as:

$$y(n) = \sum b_k x(n-k) \quad (1)$$

Here, filter output: $y(n)$, b_k:filter coefficient and $x(n-k)$: filter input delayed by k samples. The FIR filter can be designed by different windowing methods. This FIR filter has been designed by using Kaiser Window method. Kaiser window function expressed as:

$$\omega(n) = \frac{I_0(\beta\sqrt{1-(1-\frac{2n}{N-1})^2})}{I_0(\beta)} \quad (2)$$

FPGA (Field Programmable Gate Array) is a good platform for implementing signal processing algorithms because of low cost and high logic density, high computing speed, programmability and configurability.

State of Art

There have been various studies done by researchers for ECG noise removal. The Baseline Wander noise removed using FPGA based adaptive filter has been proposed in [7]. This paper presents development and implementation of architecture for a LMS (least mean square) based Adaptive filter using Spartan 3s400pq208-4 board and Xilinx system Generator (XSG) software, to minimize the Baseline wander noise (0.15 to 0.3Hz) from Electrocardiogram (ECG) signal. The signals under experiment are retrieved from MIT-BIH database and are added with Baseline Wander noise. SNR and MSE have been achieved 26.678db and 4.83 respectively [7].

A Notch FIR Filter has been proposed in [6]. The FIR filter has been design in direct form approach for the purpose of removing Powerline Interference Noise from ECG signal. This approach gives better performance than the common filter structure. The minimum power 0.073w has been achieved in FIR filter based on DA to 625 taps, 8 bits inputs input and 9 bits coefficients. This system has been designed using VHDL and implemented on Xilinx ISE Artix-7 series FPGA. Xilinx XPower analyzer used for power analyzed purpose.

The Distributed Arithmetic (DA) architecture based Finite Impulse Response Filter (FIR) has been implemented on FPGA with the help of Xilinx system generator software has been given in [8]. A multiplier less distributed arithmetic (DA) has been used for eliminating EMG (Electromyogram) noise. The filter designed with Kaiser Window which works better than other type of windowing methods (Hamming, Hanning, Bartlett) [8]. The system has been deduced hardware resources using utilization of DA FIR has been minimized [8]. EMG noise has been taken from MIT-BIH noise stress database. The simulation results have been shown that high frequency EMG noise from ECG removed effectively by using FIR low pass filter. The Xilinx chip of Spartan 3E XC3S500e-4fg320 has been used for implementation using Xilinx system generator 10.1 with Matlab version7.4.0 (2007a).

FPGA based FIR multilevel filtering for ECG de-noising has been given in [9]. The cascaded combination of digital FIR filter has been design and applied to the ECG signal. After analysis of different combination of FIR low pass, high pass and Notch filter, best SNR has been found in FIR low pass hamming, FIR high pass Rectangular and FIR Notch Rectangular combination[9]. The FIR filter combination has been designed and synthesized in MATLAB environment and implemented on a FPGA Viretex-6 device. The signal power has been observed at output end is 284.4 db. Also, the resource utilization for the cascade combination of FIR is in reasonable range and also power consumption by the various modules has been found 3.926 W [9].

MAC (multiplier and accumulator) unit has been used to design FIR filter given in [10]. This FIR filter based MAC unit has been used to suppress the PLI noise from real time ECG signal. The performance of this filter depends on the speed and power of the MAC unit employed inside the filter. It is shown that MAC is optimized for both timing and power which shows 6.2% improvement in performance and 12.1% reduction in power from other implemented designs [10]. The convergence time of the algorithm has been observed to be less than 0.2 μsec with significant power savings to improve battery life.

Different windowing methods based on FIR filter have been used for baseline wander noise has been presented in [11]. FIR filters with Kaiser Window, FIR Equiripple filter, Rectangular, Hanning and Blackman functions have been performed. After filtration spectral density has been achieved 29.57 dB/Hz using Kaiser Window. The Kaiser Window and Rectangular Window have been shown better results at the expense of some more computational load as the order of the filter is large. In case of remaining Windows i.e. Hanning and Blackman Windows, the order of filter easily grow very much high [11]. It increases the number of filter coefficients which increases the large memory requirement and problems in hardware implementation [11]. The FIR Kaiser Window filter can be best choice for the removal of baseline wandering among FIR filters [11]. In the above literature, different filtering techniques have been discussed. From the state of art, it is clear that the FIR filter gives better performance. On comparing with the windowing methods, Kaiser Window has been given better results than others. Also, FIR filter using MAC unit gives better performance in terms of speed, power and area. The cascaded FIR filter can remove different noises in a single filter.

Proposed Method

The noisy ECG database has been taken as an input. The cascaded FIR filter has been designed for de-noising purpose. The cascaded FIR filter made up of High pass filter (HPF), Band stop filter (BSF) and Low pass filter (LPF). The Kaiser Window method has been used to design FIR filter. Block diagram of Cascaded FIR filter as shown in fig. 3.

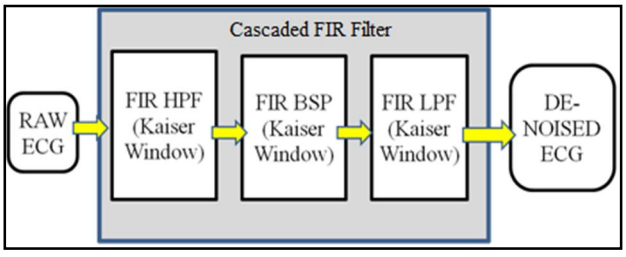

Figure3. Block Diagram of Cascaded FIR Filter [3]

Generally, the bandwidth of ECG signal is 0.1-300 Hz with amplitude of 0.1 to 4 mV [3]. This signal is affected by noise in range of frequencies. In this system, first filter is Kaiser Window based FIR HPF (High Pass Filter) which can remove baseline wander noise (0.1-0.5 Hz) from raw ECG. To get clear visualization of ECG, it is necessary to eliminate this low frequency component with cut-off frequency 0.5 Hz. After removing baseline wander noise, second Kaiser Window based FIR BSF (Band Stop Filter) has been designed for removing Power line Interference from ECG signal. This band stop filter can remove this mid frequency component with cut-off frequencies of Fc1=59.5 Hz & Fc2=60.5 Hz. At last, next filter is FIR LPF (Low Pass Filter) which is also Kaiser Window based filter. This FIR Low pass filter can suppress EMG noise (>100 Hz). Finally, a clean ECG signal has been obtained after removing high frequency component. The clean ECG signal can be used for diagnosis the various diseases.

System Implementation

This section describes proposed system implementation starting from filter design to hardware implementation. Major steps have been explained below.

Generate filter coefficient: The 'fdatool' is very useful tool in MATLAB for generating filter coefficients. The Kaiser Window method has been selected to get better performance, (value of beta has been taken 0.5), and cut-off frequency has been selected according to filter type. The fig. 4 shows 'fdatool' in MATLAB.
The Table 1 shows specification of low pass FIR filter for generate coefficient in 'fdatool'. Similar process is carried out for generating FIR high pass filter and FIR band stop filter coefficients by changing its cut-off frequency.

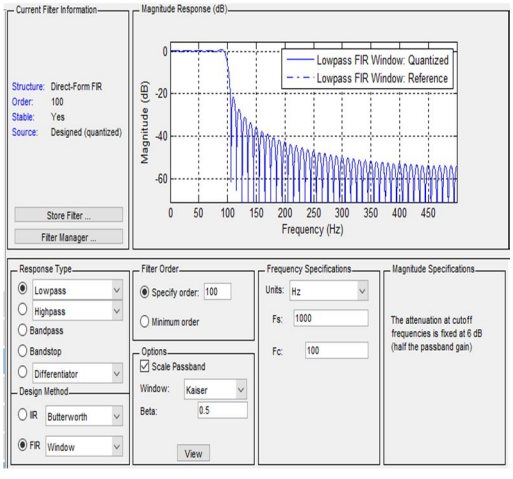

Table 1: Specification of Low Pass Filter

Filter Type	FIR Low Pass Filter
Windowing Method	Kaiser Window (beta=0.5)
Filter order	100
Sampling Frequency	1000 Hz
Cut-off Frequency	100 Hz

Figure4. 'fdatool' in MATLAB

ECG database: The noisy ECG databases have been taken from Physionet.org. There are different databases available on this site. The MIT-BIH Arrhythmia (record 100) has been selected. The given fig. 5 shows ECG database selection from physiobank.

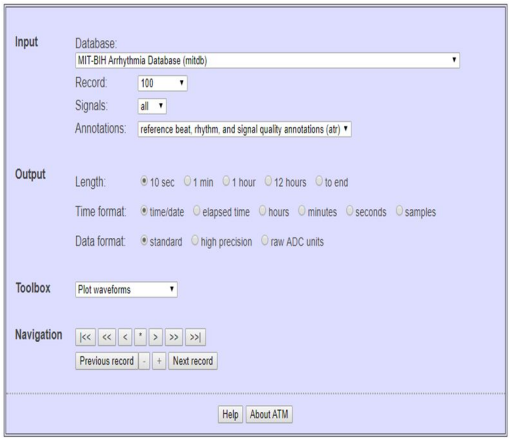

Figure5. The ECG database selection from physiobank [12]

Proposed system architecture: The given fig. 6 shows proposed system architecture. The address generator has been used for generate the address to each BRAM to get one by one sample from BRAM (Block RAM). The clock and reset are the inputs of the system. The outputs of address generator are connected to all four BRAM as shown in fig. 6. To store ECG samples one BRAM has been used. On the other hand, remaining three BRAM have been used for different filter coefficients. The ECG samples and filter coefficients have been taken in ".coe" file. The ECG data samples and filter coefficients are 16 bit. The High Pass filter has 16 × 16 bit input and 32 bit output and this output is connected to next Band Stop filter. Now, it has 32 × 16 bit input and 48 bit output and this output is connected to Low Pass filter. Finally, Low Pass filter has 48 × 16 bit input and 64 bit output. At the end filtered output samples have been obtained. Each filter block consisting MAC (multiplier and accumulator) unit as shown in fig. 6. In this system MAC unit is made up of Booth multiplier and accumulator. The architecture of MAC unit has been discussed in below:

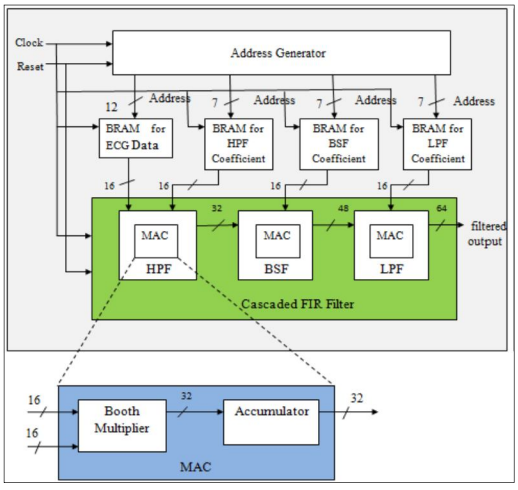

Figure 6. Proposed System Architecture

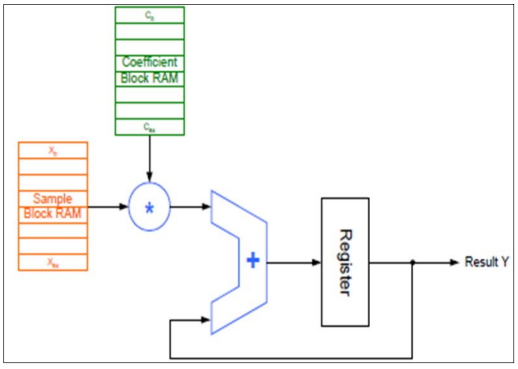

Figure 7. MAC unit structure [13]

MAC stands for multiply-accumulate unit. MAC is composed of an adder, multiplier and an accumulator. It computes the multiplication of two operands and adds with the third operand. The speed of the conventional MAC unit is optimized by using various frontline multipliers like Wallace tree multiplier, Booth Multiplier, Baugh-Wooley multiplier [14]. In this system, Booth multiplier has been used for higher order bits. There are two BRAM one is for to store ECG samples and another one is for filter coefficients as shown in fig.6. The inputs for the MAC are to be fetched from memory location and fed to the multiplier block of the MAC, which will perform multiplication and gives the result to the adder which will accumulate the result and then will get the final output.

Booth multiplier: Booths multiplication algorithms is a multiplication algorithm which can multiply two signed binary numbers in a two's complement notation. Booth's algorithm has the ability to perform fewer addition and subtractions in

comparison to normal multiplication algorithm. It is encoding processes which can be used to minimize the no. of partial products in a multiplication process. Conditions for Booth Algorithm are as follows:

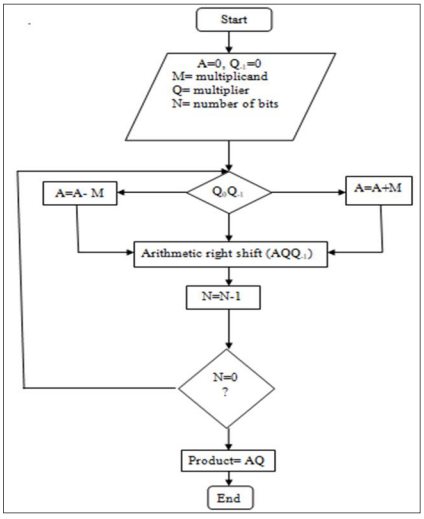

Figure8. Flow chart of Booth algorithm

Table2. Conditions for Booth's algorithm

Sr. No.	Q_0	Q_{-1}	Conditions
1.	0	0	Only shifting
2.	1	1	Only shifting
3.	0	1	Perform A+M; then shift
4.	1	0	Perform A-M; then shift

Results

The proposed filter has been synthesized in Xilinx ISE by using VHDL. In this top level entity, there are different sections or blocks such as address generator, BRAM, Cascaded FIR filter, MAC. The fig. 9 shows top level entity of the proposed system.

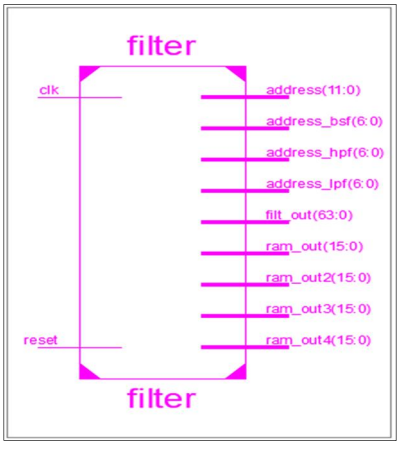

Figure9. RTL schematic of top level entity

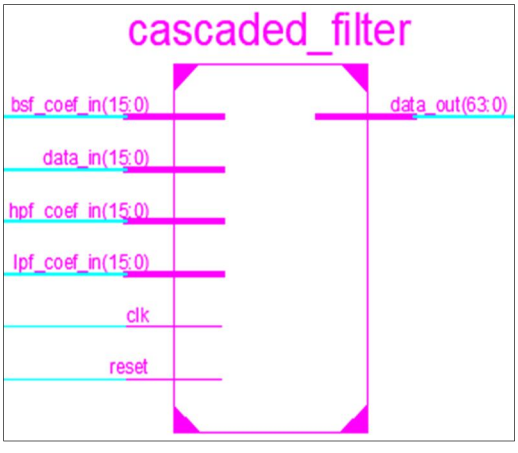

Figure10. RTL schematic of Cascaded FIR filter

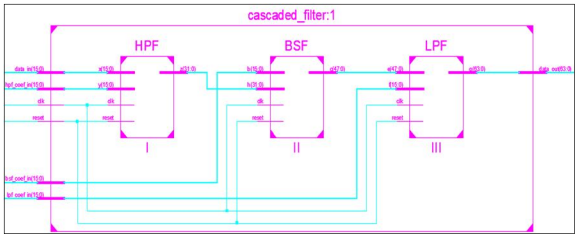

Figure11. RTL schematic of Cascaded FIR filters

Table3. Device utilization summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	274	28800	0%
Number of Slice LUTs	4892	28800	16%
Number of fully used LUT-FF pairs	143	5023	2%
Number of bonded IOBs	163	480	33%
Number of Block RAM/FIFO	4	60	6%
Number of BUFG/BUFGCTRLs	1	32	3%

Xilinx synthesis results in ISIM simulator: The Fig.12 shows output of FIR High Pass Filter in ISIM. Also, fig. 13 shows output of BSF in ISIM simulator and fig. 14 shows LPF output in ISIM simulator. Output of ISIM have been compared against MATLAB results for validation and found to be as expected.

Figure12. Output of HPF in ISIM

Figure13. Output of BSF in ISIM

Figure14. Output of LPF in ISIM

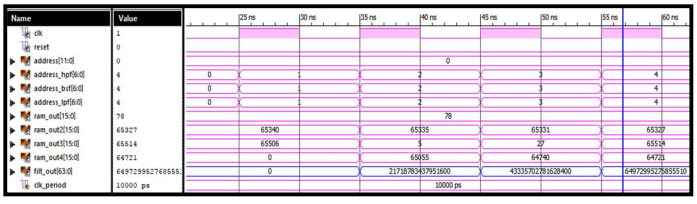

Figure15. Output of Cascaded FIR filter in ISIM

The fig. 15 shows 64 bit output of cascaded FIR filter in ISIM. There are different address generated for ram_out, ram_out2, ram_out3 and ram_out4 which are namely address, address_hpf, address_bsf, address_lpf respectively. The filt_out is denoted as final 64 bit output of the system. The table 3 shows utilization summary of the device.

MATLAB simulation results: The output samples of ISIM simulator have been plotted in MATLAB. The fig. 16 shows that Baseline Wander noise has been removed from ECG signal. Similarly, the fig. 17 shows Powerline Interference noise has been removed and the fig. 18 shows EMG noise has been removed from noisy ECG signal. The clean ECG has been given after removal of all noises as shown in figure19. The Powerline Interference noise is shown in frequency domain whereas; other waveforms have been shown in time domain.

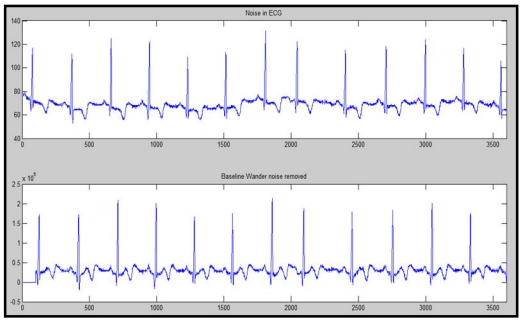

Figure16. Baseline Wander noise removed

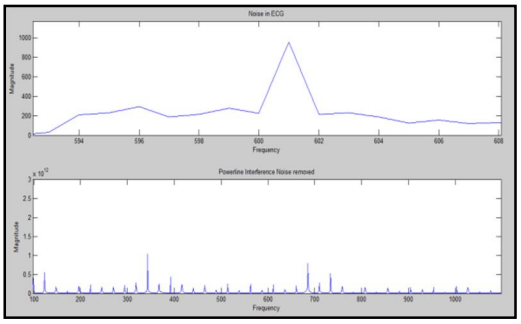

Figure17. Powerline Interference noise removed

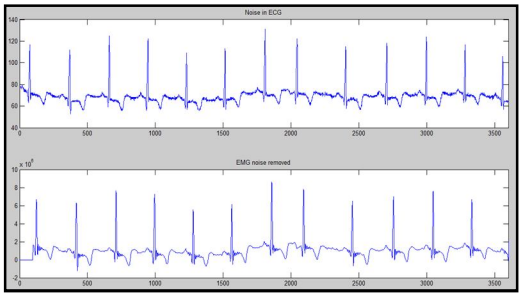

Figure18. EMG noise removed

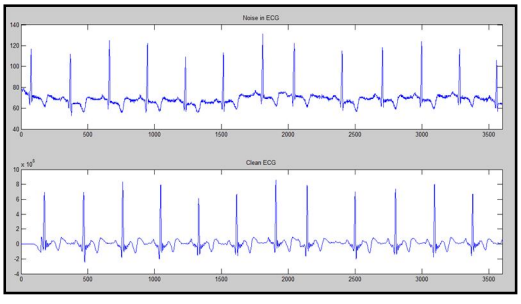

Figure19. Clean ECG

Performance measurement

Figure20. Power analyzer of Cascaded FIR filter implemented on Virtrex5

Table 4 Signal to Noise ratio calculated before and after filtration

Filter type	SNR (before filtration)	SNR (after filtration)
HPF	2.7984	3.9837
BSF	2.7984	3.9268
LPF	2.7984	3.9922
Cascaded FIR filter	**2.7984**	**5.4617**

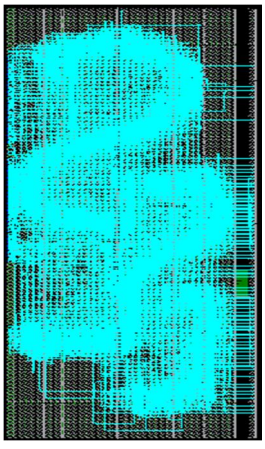

Figure21. Routed design of the proposed system

Signal to noise ratio (SNR): It is defined as the ratio of signal power to the noise power which measures the original signal corruption. A higher SNR guarantees the clear acquisitions with low distortions and artifacts caused by unwanted noise.
SNR= Psignal / Pnoise = μ/σ
Where, μ is the signal mean and σ is the standard deviation calculation of the noise. The table 4 shows that SNR calculated before and after filtration.
Power analysis: The Xilinx XPower analysis tool has been used to analyze power consumption. For the proposed system total power consumption has been found to be 0.453W for given input database and filter coefficients. The fig. 20 shows Power analyzer of Cascaded FIR filter implemented on Virtrex5 and fig. 21 Routed design of the proposed system.

Conclusion

With the propose approach, it is clear that, Baseline Wander noise, Powerline Interference noise and EMG noise have been removed and clean ECG has been obtained. These noises have been removed from ECG MIT-BIH arrhythmia database (record# 100). Also, the Cascaded FIR filter gives optimized results at an order 300. The SNR has been found to be 5.4617 after filtration. Power consumption of the system has been found to be 0.453W. By using MAC architecture utilization of hardware resources have been reduced as shown in table 3. Cascaded FIR filter has removed these noises in a single filter and gives better accuracy. The proposed work can be further improved in future to make cascaded FIR filter faster by using pipelined architecture.

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